AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior listing of claims in this application.

Claims 1-21 (Canceled).

22. (Currently amended) A transistor structure comprising:

a semiconductor substrate;

a gate stack with sidewalls provided over said substrate, said gate stack comprising:

a gate oxide layer provided [[on]] over said substrate;

a polysilicon layer provided [[on]] over said gate oxide layer;

~~at least one unetched silicide layer formed over and in contact with said polysilicon layer~~ insulating spacers;

at least one channel implant region formed underneath said gate stack, wherein said insulating spacers define at least in part the at least one channel implant region; and,

source and drain regions provided in said substrate on opposite sides of said gate stack.

23. (Currently amended) A structure as in claim 22, ~~further comprising first sidewall~~ wherein said insulating spacers are formed on the sidewalls of said gate stack.

24. (Currently amended) A structure as in claim [[23]] 22, ~~further comprising second sidewall~~ wherein said insulating spacers are provided over ~~and at edges of~~ said ~~conducting~~ polysilicon layer.

25. (Currently amended) A structure as in claim 23, ~~further comprising~~ wherein said at least one channel implant region ~~in said substrate below said gate stack, which~~ is defined at least in part by said ~~first~~ sidewall spacers and is approximately the same width as said gate stack.

26. (Currently amended) A structure as in claim 24, ~~further comprising~~ wherein said at least one channel implant region ~~in said substrate below said gate stack, which~~ is defined at least in part by said ~~second sidewall~~ insulating spacers and is narrower than the width of said gate stack.

27. (Currently amended) A structure as in claim 23, further comprising an insulating layer adjacent to said ~~first~~ sidewall spacers, said insulating layer and said ~~first~~ sidewall spacers having ~~etched out upper portions~~ at least a portion of their upper surfaces removed to define an area extending beyond a lateral width of said gate stack.

28. (Currently amended) A structure as in claim 27, ~~further comprising~~ wherein said at least one channel implant region ~~in said substrate below said gate stack, which~~ is defined at least in part by said area.

29. (Currently amended) A structure as in claim 25, further comprising second ~~sidewall~~ insulating spacers provided over ~~and at edges of~~ said ~~conducting~~ polysilicon layer.

30. (Currently amended) A structure as in claim 29, further comprising ~~at least another~~ a second channel implant region formed in said ~~substrate below said gate~~

~~stack~~ at least one channel implant region, which is defined at least in part by said second ~~sidewall~~ insulating spacers.

Claims 31-32 (Canceled).

33. (Currently amended) A structure as in claim 22, ~~wherein said~~ further comprising a silicide layer formed over said gate stack, wherein said silicide layer is formed of a material [[in]] selected from the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.

Claims 34-69 (Canceled).

70. (Currently amended) A transistor structure comprising:

a semiconductor substrate;

a gate stack with sidewalls provided over said substrate, said gate stack comprising:

a gate oxide layer provided [[on]] over said substrate;

a conducting layer provided [[on]] over said gate oxide layer;

~~first~~ sidewall spacers provided [[on]] adjacent to the sidewalls of said gate stack;

an insulating layer formed adjacent to said sidewall spacers, said insulating layer and sidewall spacers having etched out upper portions that define an area extending beyond a lateral width of said gate stack; and

at least one channel implant region ~~in said substrate below~~ formed beneath said gate stack, which is defined at least in part by said ~~first sidewall spacers~~ area, wherein said at least one channel implant region is wider in width than said gate stack[[;]]

~~at least one unetched silicide layer formed over and in contact with said conducting layer; and,~~

~~source and drain regions provided in said substrate on opposite sides of said gate stack~~.

71. (Original) A structure as in claim 70, wherein said conducting layer is polysilicon.

Claims 72-73 (Canceled).

74. (Currently amended) A structure as in claim 70, ~~wherein said~~ further comprising a silicide layer formed over said gate stack, wherein said silicide layer is formed of a material [[in]] selected from the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.

75. (Currently amended) A transistor structure comprising:

a semiconductor substrate;

a gate stack with sidewalls provided over said substrate, said gate stack comprising:

a gate oxide layer provided [[on]] over said substrate;

a conducting layer provided [[on]] over said gate oxide layer;

first sidewall spacers provided [[on]] adjacent to the sidewalls of said gate stack;

second sidewall spacers provided over ~~and at edges of~~ said conducting layer; and

at least one channel implant region ~~in said substrate below~~ formed underneath said gate stack, which is defined at least in part by said second sidewall spacers, wherein said at least one channel implant region is narrower in width than said gate stack[[;]]

~~at least one unetched silicide layer formed over and in contact with said conducting layer; and,~~

~~source and drain regions provided in said substrate on opposite sides of said gate stack~~.

76. (Original) A structure as in claim 75, wherein said conducting layer is polysilicon.

77. (Currently amended) A structure as in claim 75, further comprising an insulating layer formed adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having ~~etched out upper~~ removed portions [[to]] that define an area extending beyond a lateral width of said gate stack.

78. (Currently amended) A structure as in claim 77, ~~further comprising at least one~~ wherein a second channel implant region ~~in said substrate below~~ is formed beneath said gate stack, which is defined at least in part by said area, wherein said second channel implant region is wider in width than said gate stack.

79. (Currently amended) A structure as in claim 77, ~~wherein said~~ further comprising a silicide layer formed over said gate stack, wherein said silicide layer is formed of a material [[in]] selected from the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.

80. (Currently amended) A transistor structure comprising:

a semiconductor substrate;

a gate stack with sidewalls provided over said substrate, said gate stack comprising:

a gate oxide layer provided [[on]] over said substrate;

a conducting layer provided [[on]] over said gate oxide layer;

first sidewall spacers provided [[on]] adjacent to the sidewalls of said gate stack;

an insulating layer formed adjacent to said first sidewall spacers~~, said insulating layer and said first sidewall spacers having etched out upper portions to define~~ that defines an area extending beyond a lateral width of said gate stack;

~~at least one~~ a first channel implant region ~~in said substrate below~~ formed underneath said gate stack, which is defined at least in part by said area; and

a second channel implant region formed within said first channel implant region

~~at least one unetched silicide layer formed over and in contact with said conducting layer; and,~~

~~source and drain regions provided in said substrate on opposite sides of said gate stack~~.

81. (Original) A structure as in claim 80, wherein said conducting layer is polysilicon.

Claims 82-83 (Canceled).

84. (Currently amended) A structure as in claim 80, ~~wherein said~~ further comprising a silicide layer formed over said gate stack, wherein said silicide layer is formed of a material [[in]] selected from the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.

85. (Currently amended) A transistor structure comprising:

a semiconductor substrate;

a gate stack with sidewalls provided over said substrate, said gate stack comprising:

a gate oxide layer provided [[on]] over said substrate;

a conducting layer provided [[on]] over said gate oxide layer;

first sidewall spacers provided [[on]] adjacent to the sidewalls of said gate stack;

~~an insulating layer adjacent to said first sidewall spacers, said insulating layer and said sidewall spacers having etched out upper portions to define an area extending beyond a lateral width of said gate stack;~~

a first channel implant region formed underneath said gate stack, which is defined at least in part by said first sidewall spacers;

second sidewall spacers provided over ~~and at edges of~~ said conducting layer;

~~at least one~~ a second channel implant region ~~in said substrate below said gate stack~~ formed within said first channel implant region, which is defined at least in part by said second sidewall spacers~~;~~

~~at least one unetched silicide layer formed over and in contact with said polysilicon layer; and,~~

~~source and drain regions provided in said substrate on opposite sides of said gate stack~~.

86. (Currently amended) A structure as in claim 85, ~~wherein said~~ further comprising a silicide layer formed over said gate stack, wherein said silicide layer is formed of a material [[in]] selected from the group consisting of W, WSi_x, WN, Ti, TiN, and combinations thereof.

Claims 87-91 (Canceled).

92. (New) A gate stack with sidewalls for use in a MOSFET, said gate stack comprising:

an oxide layer provided over a semiconductor substrate;

a conducting layer provided over said oxide layer;

a first set of spacers provided on each side of said gate stack with a second set of spacers provided over said conducting layer; and

a first channel implant region formed underneath said gate stack and in said semiconductor substrate, wherein the first set of spacers or second set of spacers define at least in part the width of said channel implant region.

93. (New) The gate stack structure of claim 92, wherein said first set of spacers are formed on the sidewalls of said gate stack.

94. (New) The gate stack structure of claim 93, wherein said first channel implant region is formed self-aligned to said gate stack.

95. (New) The gate stack structure of claim 94, further comprising a second channel implant region formed within the first channel implant region, wherein said second channel implant region is narrower in width than said first channel implant region.

96. (New) The gate stack structure of claim 92, wherein said second set of spacers are formed over said conducting layer.

97. (New) The gate stack structure of claim 96, wherein said first channel implant region is narrower in width than said gate stack.

98. (New) The gate stack structure of claim 92, further comprising an insulating layer formed adjacent to said first set of spacers, wherein said insulating layer and said first set of spacers have etched out portions that define an area extending beyond a lateral width of said gate stack.

99. (New) The gate stack structure of claim 98, wherein said first channel implant region is wider than said gate stack.

100. (New) The gate stack structure of claim 98, further comprising a second channel implant region formed within said first channel implant region.